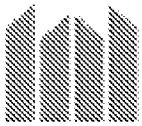

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Docket No.: 72255/00463 **PATENT**

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

FIRST NAMED INVENTOR	:	Harish R. Devanagondi **Confirmation No.: 7012**
FOR	:	MULTI-SLICE NETWORK PROCESSOR
APPLICATION NO.	:	10/612,889
FILING DATE	:	July 3, 2003
EXAMINER	:	Jianye Wu
ART UNIT	:	2616
CUSTOMER NO.	:	**23380**

AMENDMENT

FAXED TO (571) 270-2665
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

Please amend the above-identified application as follows:

Amendments to the Claims are reflected in the listing of claims which begins on **page 2** of this paper.

Remarks/Arguments begin on **page 13** of this paper.

Amendment to the Claims:

This listing of claims will replace all versions, and listings, of claims in the application:

Listing of Claims:

Please cancel claims 1-21

22. (New) In a multi-slice network processor system comprising a plurality of processing slice modules, each module processing and storing a slice of packet data, a method for processing a packet in packet slices for transfer over a network interface comprising:

prepending a system header to the packet, the system header providing information for use by the multi-slice system, the information comprising a sequence number;

assigning a packet identifier to the packet;

segmenting data of the packet into cells, the data including both header and body data for the packet;

generating cell descriptive information for each cell, the cell descriptive information including the packet identifier, and a packet position indicator indicating an order position of data of the cell with respect to the packet;

delivering one or more cells of the packet to one or more processing slice modules based upon load balancing criteria;

storing one or more cells in a buffer in the packet slice;

generating a buffer correlation data structure correlating the buffer of the packet slice to the packet, wherein the buffer correlation data structure is a linked list of buffer identifiers;

maintaining an independent set of upper bits of a sequence number for each communication flow; and

~~responsive to detecting one of the processing slices delivering a sequence number that is smaller in value than an immediately preceding sequence value for the same slice,~~ incrementing the independent set of upper bits for the respective communication flow, concatenating the set of upper bits with a set of bits of ~~the~~ a sequence number in the system header into an index, indexing into a re-sequencing buffer space of sufficient depth to cover a slice-to-slice skew case based on the index, and resequencing the packet into its sequence order position responsive to

one of the processing slices delivering a packet having a sequence number that is smaller in value than a sequence number for an immediately preceding packet for the same slice,.

23. (Previously Presented) The method of claim 22 wherein load balancing criteria includes that no load balancing is in effect.

24. (Previously Presented) The method of claim 22 wherein the packet identifier is a sequence number representing an order of the packet in a communications flow and further comprising assigning a communications flow indicator to the cell descriptive information of each cell of the packet.

25. (Previously Presented) The method of claim 22 wherein the cell descriptive information further comprises a slice position indicator indicating an order position of the data of the cell with respect to a slice of data of the packet.

26. (Previously Presented) The method of claim 25 further comprising delivering body data of the packet to one or more of the processing slices ahead of the header data of the packet.

27. (Previously Presented) The method of claim 26 further comprising:

performing lookup functions for each slice of data;

determining a size of data change in header data; and

communicating the size of data change to a queue manager via an indicator in the system header.

28. (Previously Presented) The method of claim 22 further comprising generating a slice correlation data structure for the packet including a packet reference pointing to the buffer of the packet slice including the first cell of the packet, and a respective buffer indicator for the buffer in each packet slice storing the first cell in the slice for the packet.

29. (Previously Presented) The method of claim 28 further comprising entering the slice correlation data structure as a single queue entry into a queue.

30. (New) A multi-slice network processor system comprising:

a plurality of parallel processing slices, each processing slice comprising a lookup processing module and access to a storage sub-system, the storage sub-system including a memory, the memory storing at least one group of cells of a packet in a buffer; and a buffer manager, the buffer manager maintaining a buffer correlation data structure for correlating one or more buffers to the packet, wherein the buffer correlation data structure is a linked list of buffer identifiers, the buffer correlation data structure being stored in the memory;

a network data distribution and aggregation module for segmenting a packet received from a network into one or more packet slices, the network data distribution and aggregation module having a communication interface to each of the processing slices for communicating each packet slice;

each of the plurality of slices having a channel communication interface with the network interface over which each packet slice is directed to a destination processing slice across the network interface; and

a queuing module having an enqueuing communication interface and a de-queuing communication interface with each of the processing slices, the queuing module controlling the enqueuing and dequeuing of each of the packet slices, and determining the destination processing slice based on load balancing criteria;

wherein the queuing module is configured to maintain an independent set of upper bits of a sequence number for each communication flow;

wherein the queuing module is configured to acquire a sequence number for a packet delivered from a slice; and

wherein the queuing module is configured to increment the independent set of upper bits for a communication flow, concatenate the set of upper bits with a set of bits of the sequence number of the packet into an index, index into a re-sequencing buffer space of sufficient depth to cover a slice-to-slew case based on the index, and re-sequence the packet into its sequence order position responsive to detecting one of the processing slices delivering a packet with a sequence number that is smaller in value than a~~n immediately preceding~~ sequence ~~value~~ number for a packet immediately preceding the packet for the same slice.

31. (Previously Presented) The system of claim 30 wherein load balancing criteria includes no load balancing.

32. (Previously Presented) The system of claim 30 wherein the network interface is a switch fabric, and wherein each channel communication interface comprises a port connection with the switch fabric.

33. (Previously Presented) The system of claim 30 wherein the queuing module includes a queuing memory space, the queuing module maintaining a slice correlation data structure for correlating one or more slices of the same packet slice in a single queue entry, the slice correlation data structure being stored in the queuing memory space.

34. (Previously Presented) The system of claim 30 wherein the buffer manager comprises an ingress buffer manager including an ingress buffer memory space for each processing slice, the ingress buffer memory space for storing cells received from the respective processing slice, and an egress buffer memory space for each processing slice, the egress buffer memory space for storing cells received from the switch fabric for each respective processing

REMARKS/ARGUMENTS

The Applicant acknowledges, with thanks, the telephone interview on 24 September 2008. This amendment is responsive to the telephone interview of 24 September 2008. By this amendment, claims 1-21 have been canceled without prejudice or disclaimer. Claims 22 and 30 have been amended. Reconsideration of this application as currently amended is requested.

Conclusion

If there are any fees necessitated by the foregoing communication, the Commissioner is hereby authorized to charge such fees to our Deposit Account No. 50-0902, referencing our Docket No. 72255/00463.

Respectfully submitted,

Date: September 26, 2008

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